

**IN THE ABSTRACT**

Please revise the Abstract as follows:

A (PLL) frequency synthesizer comprising: 1) a VCO that generates a first clock having frequency,  $F_{out}$ , determined by a loop filter control voltage; 2) a first divider for dividing  $F_{out}$  by  $N$  to produce a second clock of frequency,  $F_{out}/N$ ; 3) a second divider for dividing a reference frequency,  $F_{in}$ , by  $M$  to produce a third clock of frequency,  $F_{in}/M$ ; 4) a phase-frequency detector for comparing the second and third clocks, generating an UP signal if the second clock is slower than the third clock, and generating a DOWN signal if the second clock is faster than the third clock; 5) a charge pump that receives the UP and DOWN signals and increases or decreases the control voltage on the loop filter by injecting or draining a charge pump current,  $I_c$ ; and 6) a loop response control circuit for adjusting  $I_c$  as a function of  $N$  and  $M$ .